Abstract

The distinctive switching spikes seen in single memristor circuits can be suppressed in networks of memristors. Instead oscillatory behaviour interrupted by spontaneous irregular bursting spike patterns are observed. An investigation of two and three memistor circuits was undertaken to elucidate the origin and nature of these rich dynamics. No spiking or oscillations are seen in circuits where all the memristors are arranged with matching polarity. Spiking is seen in circuits where memristors are arranged anti-parallel. These dynamics may be due to increased sensitivity to initial conditions or deterministic chaos and are potentially useful for neuromorphic computing.

Observation of Spontaneous Bursting Spike Patterns Simple Three Memristor Circuits

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1 Introduction

The memristor is the fourth fundamental circuit element which was predicted to exist from symmetry arguments in 1971 [1]. It is a two terminal passive device. It is stateful and the internal state is related to past history of the device. Because of the memristor's ability to learn it has been proposed that the memristor could be a route to neuromorphic or brain-like hardware [2]. As the achievement of this is widely anticipated to lead to a step-change in not just computing, but science and even society itself (if it works we would be able to make a true machine intelligence which could enable us to answer fascinating philosophical questions about the nature of consciousness, intelligence and mankind).

The relation between memristors and neuromorphic computing dates back to 1976 when Chua and Kang expanded the idea of the memristor to a memristive system (two state variables rather than one) and suggested that the Hodgkin-Huxley model of the nerve axon could be improved by in incorporating memristors in place of the non-linear time dependent resistors [3]: an idea that wasn't demonstrated until 2012 [4], [5]. Meanwhile the scientific community has concentrated on the idea of using memristors as synapses rather than axons: simulations have shown that memristive connections could be used to reproduce spike-time dependent plasticity [6] (the process by which synapses adjust their connection weight to implement Hebbian learning [7]) and even implemented as synapses in evolved spiking networks simulations [8]. Recently, it has been noted that both our and other group's memristors possess a current-spike response to a change in voltage [9]. Thus we thought that memristors ought to be able to replicate neuronal architecture and produce dynamics associated with neurons, such as brainwaves or spike trains.

Once we decided to stop investigating the mechanism and behaviour of single memristor circuits and start building more complex systems an obvious area of interest is to examine the circuits that theorists and simulationists have designed for memristors; overwhelmingly simulationists have been interested in Chua circuits. The original Chua circuit [10] was created to demonstrate that chaos was a real phenomena and not merely due to rounding errors in the computer simulations. Furthermore, it has been suggested [5] that neurons are poised at the edge of chaos. And thus, in trying to make neuromorphic circuits, it is worth investigating both complexity and chaotic dynamics. There have been a plethora of different versions and alterations, as summarized in [11]. However,

Chua's circuit is the simplest built electronic circuit that can exhibit chaotic behaviour [12]. This circuit consists of one inductor, one resistor, two capacitors and a component called Chua's diode which is a non-linear circuit element usually fabricated from several other circuit components including op amps.

Itoh and Chua were the first to replace Chua's diode with a memristor [13]; they worked with the concept of an active memristor. A memristor is a passive device, but a circuit of a negative resistance and memristor can be viewed as an active memristor, because the negative resistance is an op-amp powered by a battery and it is the battery that adds energy to the circuit. By replacing Chua's diode with an flux-controlled active memristor they made several of chaotic oscillator circuits.

There have been many papers since detailing the rich behaviour and chaotic properties of Chua circuits containing memristors (eg. [14], [15], [16] and [17]) but these simulations all used Chua's equations for the perfect theoretical memristor and the electronic experiments replaced the memristor with a circuit equivalent, presumably due to the difficulty in obtaining an actual memristor to use. A step forward in the direction of real world functionality was Buscarino's paper [18] where Chua's diode in Chua's circuit was replaced with a pair of memristors modelled using Strukov et al's phenomenological model [2] which is based on real world measurables. The resulting simulation demonstrated chaotic behaviour. This paper used a pair of Strukov memristors connected in anti-parallel to give a symmetrical I-V curve as a replacement for Chua's diode. They then used a voltage frequency that put the memristor up to its limits to introduce asymmetry and richer behaviour. Questions could be asked as to whether the chaotic behaviour they observed in their simulations arose from the memristors or from the interaction of the errors in the model, which (even with windowing functions) is weakest at the edges of the memristor. Despite this, paper [18] represents an important step towards modelling real world memristor systems.

Another area of interest is how few components a chaotic circuit can be made with. A recent paper [19] suggested that the simplest circuit capable of producing chaos could be made with three components: a capacitor, an inductor and a memristor. HP have created what they term a neuristor, which is circuit of two memristors and two capacitors (and a load resistor) which they stated gave 'brainwave'-like dynamics from a constant voltage source (unpublished talk [20]). This circuit also had the memristors in anti-parallel.

Thus, circuits involving memristors, capacitors and inductors look likely to product interesting dynamics. According to Chua [1] the linear combination of memristors in a circuit with only one input and one output to that circuit is indistinguishable from memristor, i.e. the memristors add up in series and in parallel similarly to resistors, which would suggest that a circuit made up of only memristors would be a trivial and boring circuit (A 1-port containing only memristors is equivalent to a memristor [1]).

From behaviour observed in our lab [9] we decided to test combinations of memristors in circuits as we expected this might give rise to rich enough behaviour that we wouldn't need further complications of adding in capacitors or op amps or other circuit elements.

In this paper we are interested in a neuromorphic computing and possible appearance of chaotic behaviour. Therefore we shall do a study on the effects of interacting memristors using real world memristors. Our memristors

are titanium dioxide sol-gel memristors based on [21] as described in [22] [23]. As explained in [23], our Al-TiO_2-Al memristors come in two types: A. curved memristors which are non-linear over their whole voltage range and B: triangular memristors which have an Ohmic low resistance state. The curved memristors are thought to operate by a bulk mechanism and are closer to Chua's theoretical memristors. The triangular memristors are thought to to operate via a filamentary mechanism and are memristive systems where the second state variable is the connection state of the filament [24].

By using real world memristors we are able to make use of the memristor's actual behaviour, whereas theoretical models of the memristor are less useful in this regard as the utilisational behaviour can be abstracted out or the utility may arise from erroneous theoretical assumptions rather than the memristors true behaviour.

We shall investigate how pairs of memristors interact and test Chua's assertion that two memristors in series (or parallel) addressed only by their joint one port entry (ie there is one wire coming out and going in to that part of the circuit) are indistinguishable from a single memristor with a memristance value calculable by standard series and parallel resistor adding rules. We will look at several different three memristor circuits.

2 Methodology

All experiments were performed with a Keithley 2400 Sourcemeter. For the $I-t$ curves, the memristor circuits were taken to +0.4V for 1000 timesteps or 1.06s, the voltage source was then switched the 0V and data gathered for a further 100 timesteps. For the slow I-V test, a sinusoidal voltage of 1600 timesteps of 2s was used to see how the system would response to a slow change. Voltages were kept very low to avoid the creation of filaments via Joule heating which would lead to filamentary memristors switching into lower resistance states.

3 Single Memristor Circuits

The current response of a typical memristor to constant voltage is given in figure 1. For this experiment the memristor was taken to the test voltage at 0 seconds and the current recorded as the memristor 'equilibrated'. This was done for two voltages, +1V and -1V. There is assymmetry in the spike responses as the memristors are asymmetric.

When voltage is changed we expect a current spike, as this has been seen in all our tests [9] and this is the D.C. action of memristors (forthcoming paper). For the long time experiments shown later in this paper, the single memristor response is shown in figure 2. The spike from the original voltage switch occurs at the start, and then negative spike at 1000 timesteps that results from the change from +0.4V→0V can be clearly seen. The signal from the middle section is blown up in figure 3 to show the quality of the noise; there are no oscillations or large spikes (the spike at the end is the switching spike of the voltage source being turned off).

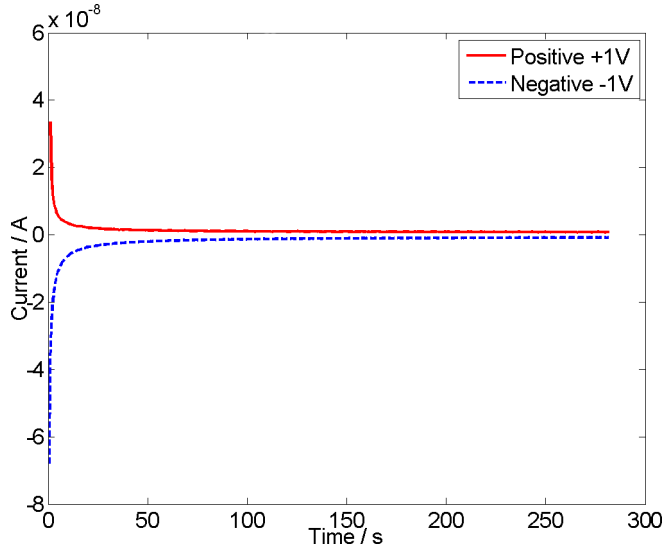

Figure 1: Memristor response under both positive and negative voltages. The voltage is switched on at 0 seconds, causing the current spike, which then equilibrates. The voltages are +1V and -1V.

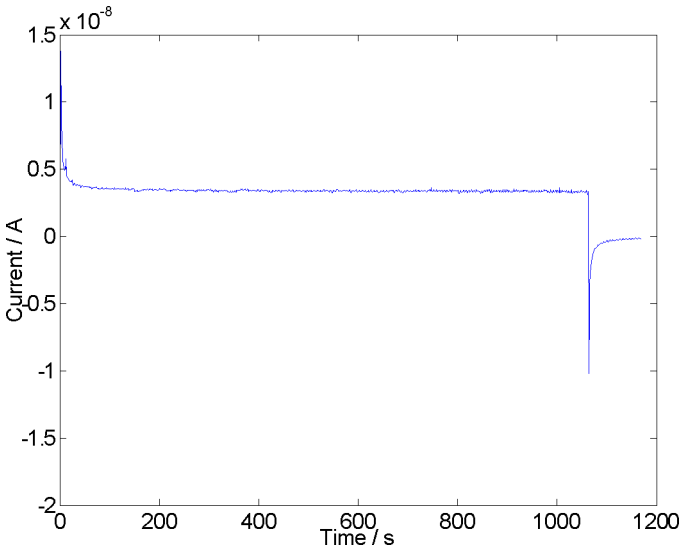

Figure 2: A single memristor response. The voltage (+0.4V) is turned on at t=0s, causing a positive current spike, and turned off at 1064s, which causes a negative current spike. These current spikes are a feature of memristance.

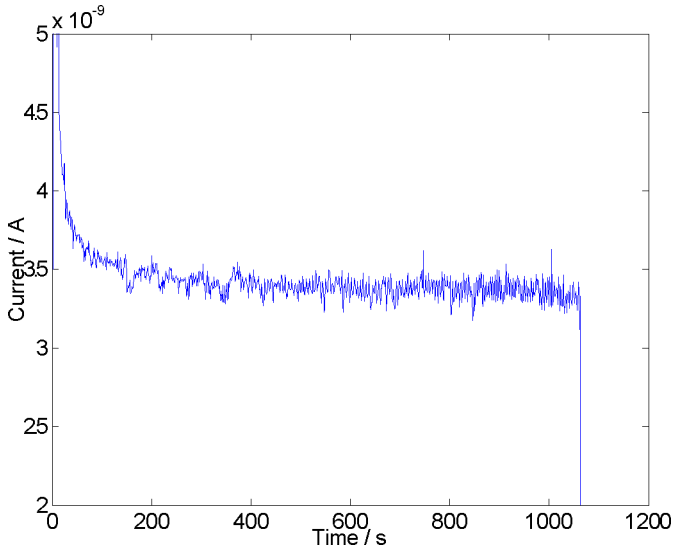

Figure 3: A close up of the $I - t$ plot in figure 2 to show the character of the noise from a single memristor.

4 Three Memristor Circuits

A dynamical system can exhibit chaotic behaviour if it has at least three state variables, so we chose to create a circuit with three memristors, which gives us the following three separate state variables, the current through the circuit, and the voltage across two of the memristors (the third being determined by the other two in a system kept at a constant voltage). In order to maximise the compositional complexity of the circuit, the memristors were wired up, two in series in reversed order, with one in parallel to the two in series as shown in figure 4. This gives us a circuit with two anti-parallel interactions. It was thought that the memristors would spike with the change of voltage and this would cause a change in resistance within a single memristor, which, with this circuit set-up would lead to a voltage change across the other memristors and thus further spikes. We used filamentary memristors for this circuit.

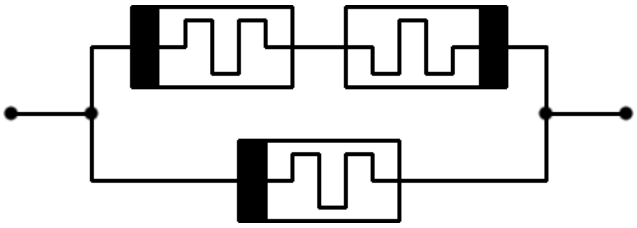

Figure 4: A three memristor circuit with two opposite polarity interactions and one same polarity interaction.

Typical results for this circuit are given in figure 5. Comparing this with the expected curve in for one memristor shown in figure 2, it shows quite a few differences. The large spike at the start has vanished, as has the one at

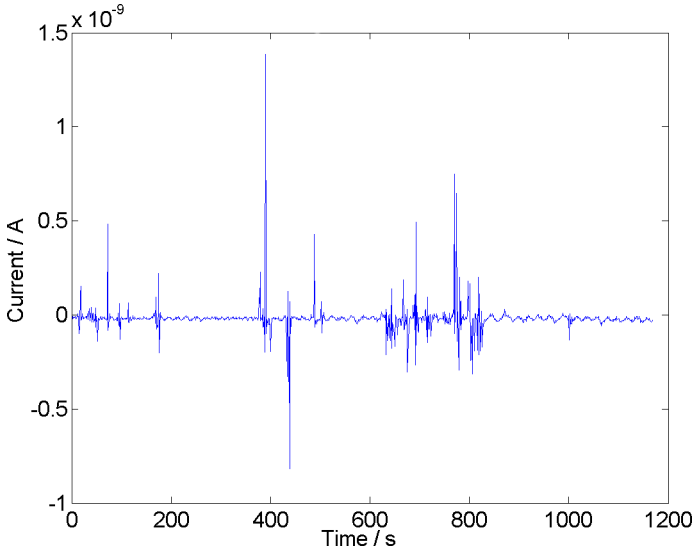

Figure 5: The current response for the three memristor circuit shown in figure 4. There seems to be an oscillatory behaviour as well as periods of spiking that resembles spike-trains in neural networks.

the end. We see oscillations in the base line, with spontaneous spiking overlaid over the top. Figure 7 shows a later run where we see sections of oscillations of different frequency. Several runs of this circuit were done to see if there was a repetition in the spiking pattern and thus if the circuits were following an long-term periodic dynamics, this was not the case.

Attempts to effect this oscillation by running a very slow $I-V$ curve is shown in figure 6 (the whole data is for one period). This does not show the expected response for a single memristor, or any change in the 'baseline' as a result of the changing voltage. The expected spikes from the one memristor circuit have been suppressed or delayed. The frequency of the baseline oscillations seems more regular than for the constant voltage.

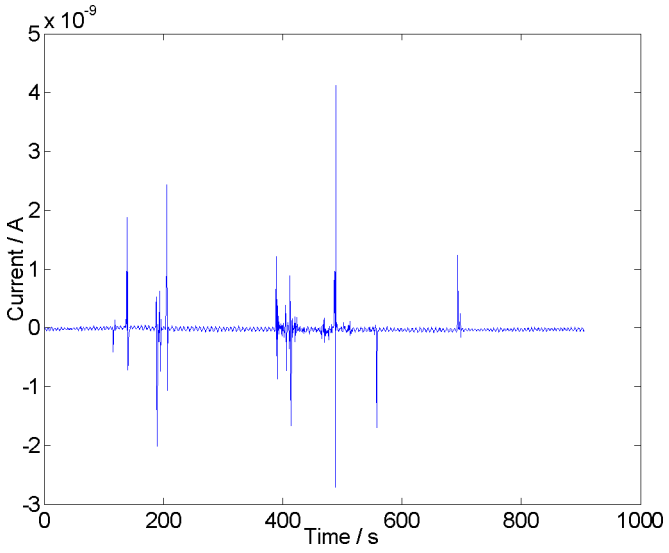

Figure 6: An I-t curve for a very slow sinusoidally varying voltage.

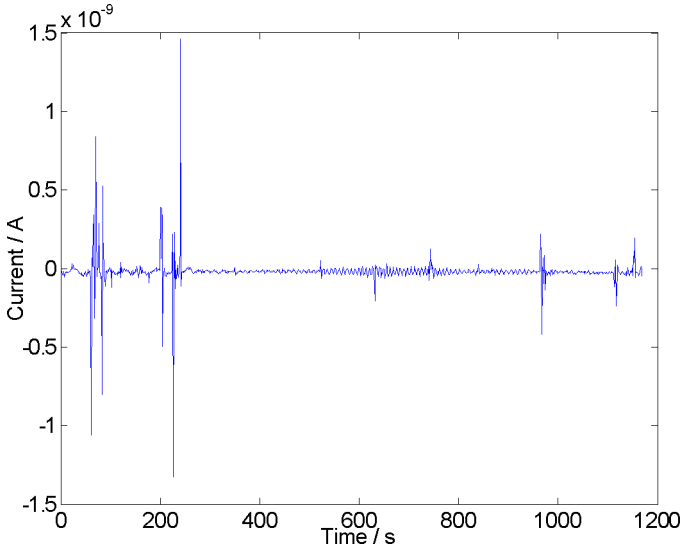

Figure 7: Another typical $I - t$ profile for the circuit shown in figure 4.

5 Two Memristor Circuits

To try and understand this, two 2 memristor circuits which are sub-circuits of the 3 memristor circuit were made. Figure 8 shows the series circuit with two memristors wired up with opposite polarity, and the $I - t$ curve is shown in figure 10. This has some spikes, faster oscillation but a very low current. Figure 9 shows two memristors in parallel and the $I - t$ curves are shown in 11, this has a higher current. These data show that two memristor circuits can produce rich behaviour with spikes and oscillations, however the behaviour is not as rich with two memristors.

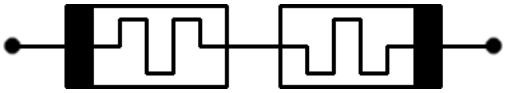

Figure 8: Two memristors in series with the the opposite polarity.

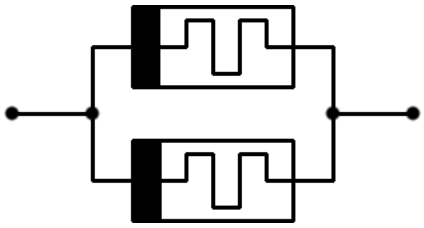

Figure 9: Two memristors in parallel with the same polarity.

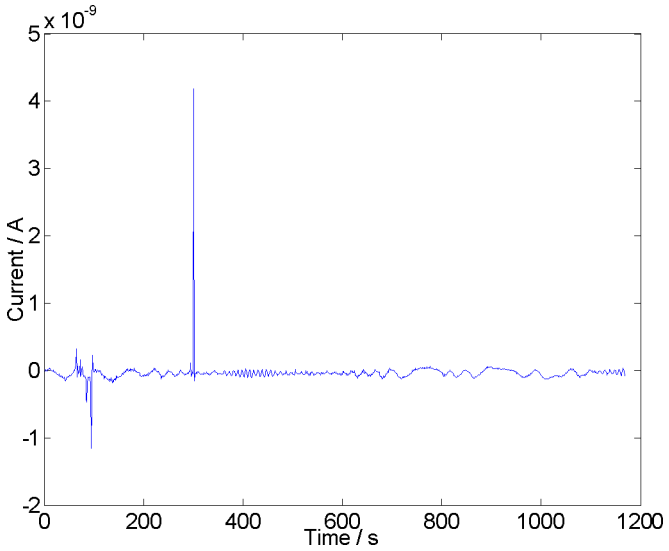

Figure 10: Two triangular switching memristors in parallel.

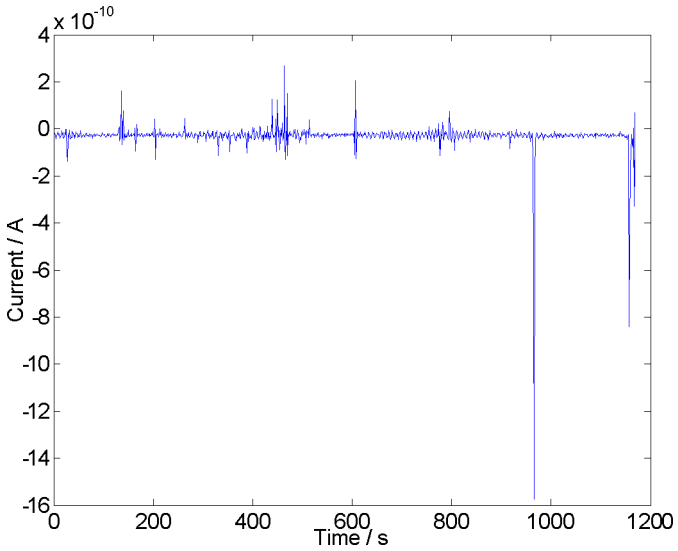

Figure 11: Two triangular switching memristors in a series circuit wired up with opposite polarity.

6 Testing Memristor Circuit Rules Using Curved Memristors.

Does this mean that memristors do not add up as expected? Not necessarily. We decided to repeat the tests with three curved memristors which are closer to the theoretical perfect Chua memristors (type A from paper [23]). We specifically chose three memristors that had similar looking $I-V$ curves that operated over a similar current range to try and decrease the compositional complexity of the circuit.

For these memristors, we found that three memristors in a circuit wired up with the same polarity, as shown in figure 12, behave qualitatively just like one memristor, see figure 14. Figure 15 shows the same memristors with the circuit diagram as shown in figure 13: this arrangement has decreased the compositional complexity by removing the anti-parallel interaction between the memristors in series and thus is equivalent to two memristors in anti-parallel. In figure 15 we see occasional switching events with a decay which strongly suggests that the more event rich behaviour seen in the other memristor systems are to do with interacting switching spikes.

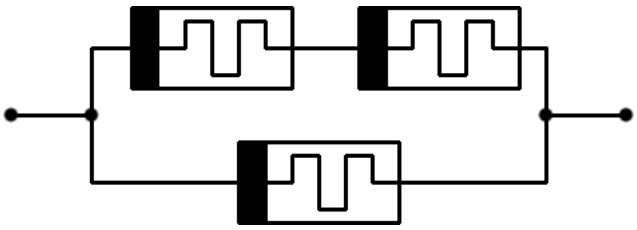

Figure 12: Three memristor circuit with all the memristors wired up with the same polarity. There is no difference between this circuit and an equivalent single memristor.

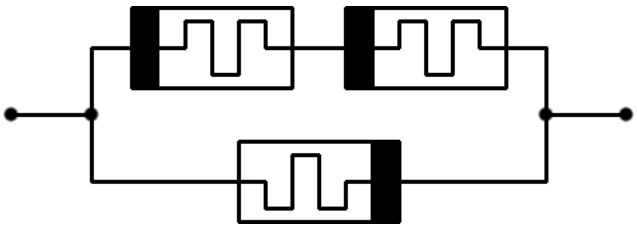

Figure 13: Three memristor circuit with only the one in parallel with the opposite polarity.

We decided to investigate the same two memristor tests as before. The parallel memristor configuration (see figure 9) is shown in figure 16 there is noise, possibly some oscillations and some spiking events. The two memristors in series (see figure 8) give the $I-t$ behaviour shown in figure 17 which is almost functionally the same as a single memristor. Thus, we conclude that 2 memristor in parallel has more compositional complexity than two memristors with opposite polarity in series.

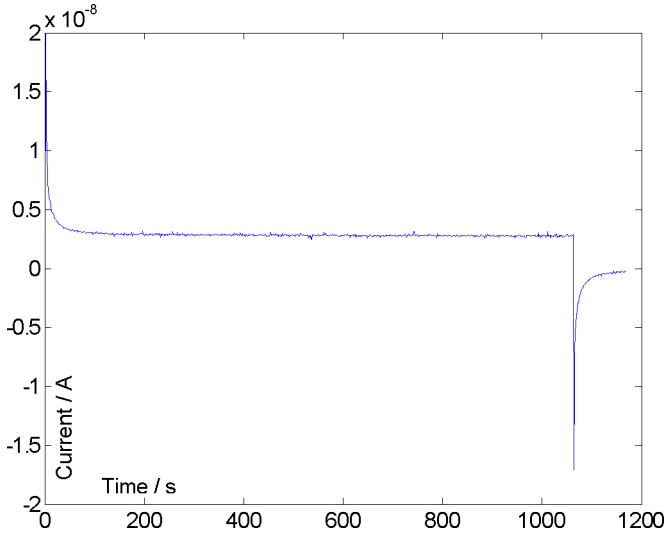

Figure 14: Three memristors set up as for figure 4 except that all the memristors are wired up the same way round. This shows that without the anti-parallel wiring, the memristors do not interact.

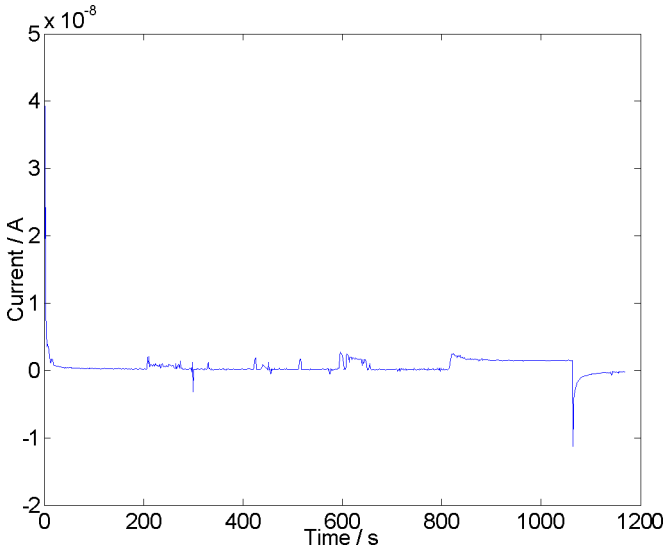

Figure 15: Two memristors in series wired up opposite direction to the one in parallel.

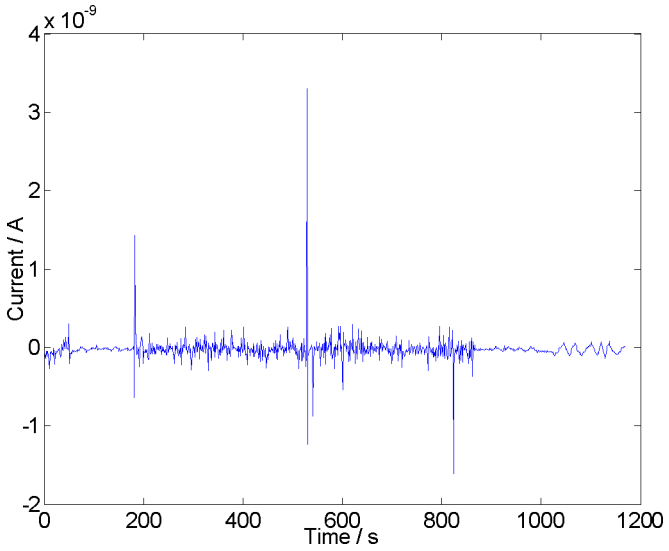

Figure 16: Two D-series memristors in parallel, same direction, as shown in figure 9

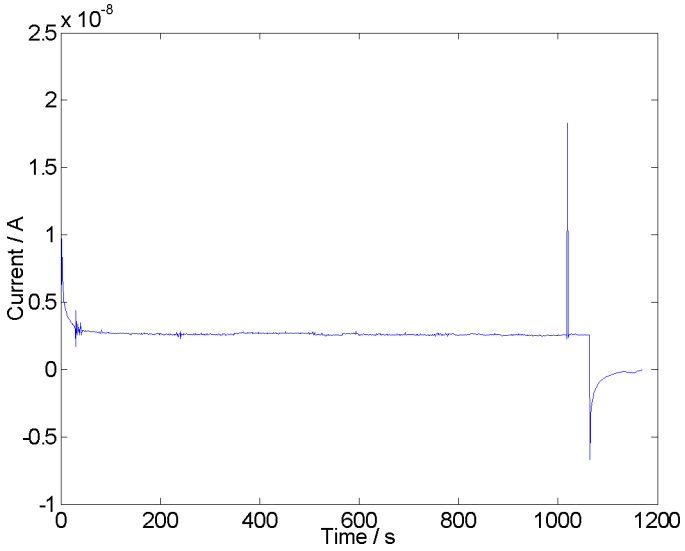

Figure 17: Two D-series memristors in series, opposite direction as shown in figure 8

7 Discussion

We have shown that three memristors can produce rich behaviour, including brain-wave-like oscillations and spiking events. An interesting question is where has the large spike at the start gone and where have the switching spikes expected from the I-V curve gone. We believe that the energy of the current spike, in fact the current itself, has been 'absorbed' into the memristor network and is the cause of the latter spiking events.

We have shown that for two or three memristors that are very similar to each other and wired up with the same polarity, Chua's prediction that they would behave exactly like a single memristor is true. We have also shown that when there is either parallel interaction or a polarity difference between the memristors, there is a higher chance of richer behaviour. From these circuits it is apparent that the circuit fragment of two memristors in antiparallel (i.e. in parallel with opposite polarity) has the highest chance of neuromorphic-like rich dynamics. This is supported by the results reported in the literature and suggests that the theoretical results reported in [18] are due to the fact their Chua circuit possesses two memristors in anti-parallel rather than a problem with the model.

The background oscillations are interesting. Although they could be dismissed as sampling noise or background noise, we do not believe this to be the case as they are not seen in the single memristor circuit and are several orders of magnitude above what would be expected on the experimental set-up used. They could be some low level emergent phenomena related to the spikes. Instead, we think it's to do with the movement of the boundary, $w(t)$. These 'waves' appear similar to that of interacting oscillators, and thus we think its potentially related to the boundary which may be oscillating due to the movement of ions around the dynamic equilibrium point, and it is this behaviour that adds up and interacts in the circuit with more than one memristor in it.

8 Further Work

This letter represents preliminary work in this area. Although the dynamics look rich, we need to do further analysis to discover what is the cause of this behavioural richness, quantify it and test whether the trajectory is genuinely chaotic. We are currently undertaking further investigations, both experimental and theoretical, into the mechanism of this behaviour.

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